A 94-GHz Monolithic Balanced Power Amplifier Using 0.1-μm Gate GaAs-Based HEMT MMIC Production Process Technology

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***Abstract*— A monolithic W-band two-stage balanced power amplifier has been developed using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic T-gate power HEMT technology. This monolithic power amplifier has demonstrated an output power of 102 mW and a small signal gain of 9 dB with input/output return losses of better than 10 dB at 94 GHz. Moreover, this monolithic chip is fabricated using production GaAs-based HEMT MMIC technology and a good yield is obtained. The circuit design relies on extensive EM analysis of matching structures and accurate device modeling. The success of this monolithic circuit development indicates the maturity of power HEMT MMIC technology at W-band.**

I. Introduction

GREAT effort has been devoted to GaAs-based HEMT MMIC technology in the past few years for millimeter-wave (MMW) applications. However, in order to insert the MMIC into systems, the R&D MMIC process technology must be transferred into production for reliability and volume concerns. For the frequency from Ka- (35 GHz) to V-band (60 GHz), various successful MMIC's, including both low noise and power applications, have been demonstrated using 0.15-μm or longer gate AlGaAs/InGaAs/GaAs pseudomorphic (PM) HEMT MMIC qualified production process [1]–[3]. At W-band, MMIC's using 0.1-μm passivated production GaAs-based low noise HEMT MMIC process have also been reported [4]–[6]. Recently, we have successfully transferred the W-band HEMT MMIC process to our production line and demonstrated an output power of more than 100 mW for monolithic power amplifiers (PA's) at 94 GHz.

This paper presents the development of this 94-GHz monolithic PA. This two-stage balanced PA has a measured output power of 102 mW at 3-dB compression with a small signal gain of 9 dB at 94 GHz. The HEMT devices used in the PA is passivated by Si_3N_4 for reliability concern and the output device periphery is 640 μm. The output power performance rivals the previously reported best W-band monolithic PA [7], which utilizes the same output device size of unpassivated HEMT devices in R&D laboratory. Moreover, a sampling of 37 sites of this PA over six wafers have been tested for gain performance, and showed an RF yield of 37% by using the 7-dB small signal gain criteria from 92–96 GHz, and good uniformity from wafer to wafer is observed. The success of this monolithic circuit development indicates the maturity of 0.1-μm power HEMT MMIC technology and the readiness of the MMIC insertion into various W-band systems with high reliability and low cost.

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II. Device Characteristics and Modeling

The W-Band HEMT structure is grown using molecular beam epitaxy (MBE) on 3-in. substrates and uses a PM $In_{0.22}Ga_{0.78}As$ channel. The HEMT device structure is based on a double heterostructure design originally developed for high-efficiency V-band power HEMT's [8] and modified to achieve a high aspect ratio for 0.1-μm gate lengths. The 0.1-μm W-band HEMT fabrication sequence shares many of the same process steps as the 0.2-μm gate length low noise and 0.15-μm gate length power HEMT production MMIC processes, ensuring high producibility [9]. The devices are passivated with PECVD silicon nitride for good reliability and robustness. Extensive characterization and statistical process control are employed for material analysis, electron beam lithography, metal-insulator-metal (MIM) dielectric thickness and capacitance, metal thickness, linewidth, and resistivity, and dc and RF device electrical parameters. This device typically exhibits a gate-to-drain breakdown voltage of 6 V measured at a gate current of 0.1 mA/mm, a peak dc transconductance of 600 mS/mm, a maximum current of 600 mA/mm, a unit current gain frequency f_T of 110 GHz, and a maximum oscillation frequency f_{max} of greater than 250 GHz at 2-V drain bias.

The HEMT linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal S-parameters to 50 GHz. These parameters are consistent with an estimation based on device physical dimensions and parameters. The Curtice-Ettenberg FET asymmetric model was used to describe the HEMT device nonlinear behavior. The nonlinear transconductance coefficients were then obtained from fitting the dc-IV measurement of the devices.

III. Circuit Design

Fig. 1 shows the the chip photograph of the monolithic PA with a chip size of 4.4 $\times$ 2.4 mm^2. The PA is a two-stage

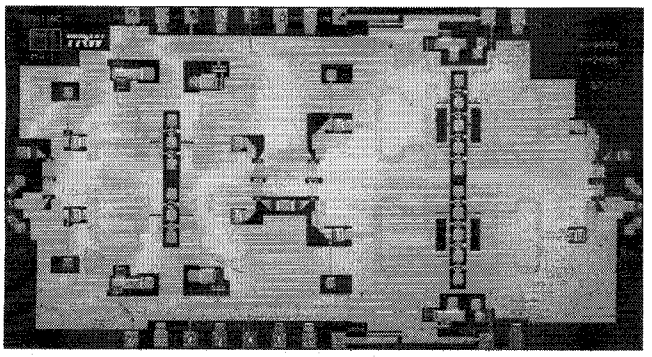

Fig. 1. The photograph of the W-band monolithic balanced power amplifier.

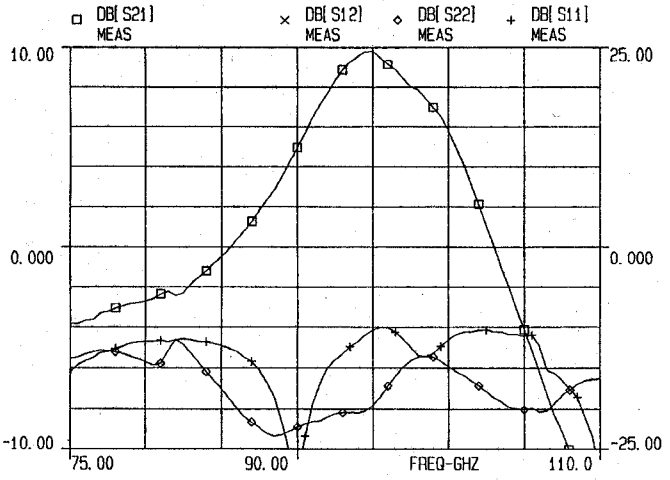

Fig. 2. The measured small signal gain plot versus frequency of the W-band monolithic power amplifier.

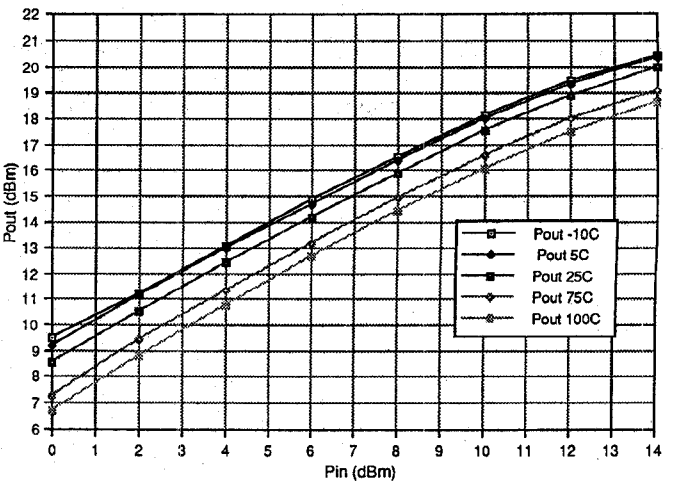

Fig. 3. The output power versus input power plot at 94 GHz from −10° to 100°C.

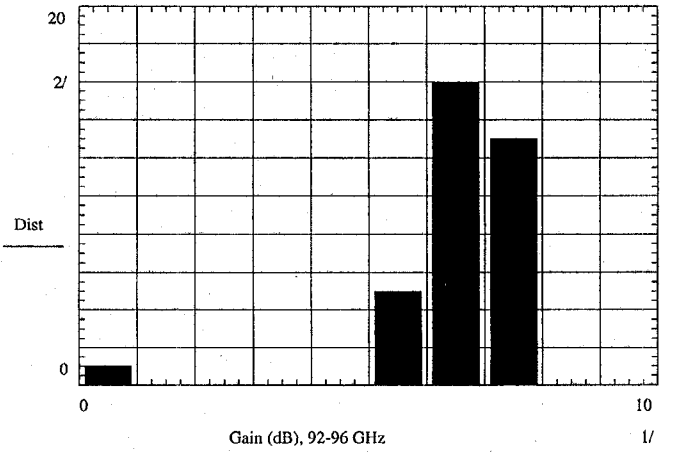

Fig. 4. The small signal gain histogram of 37 W-band monolithic PA circuits over six wafers.

design by cascading two single-stage balanced amplifiers. The first stage has a 320-μm total gate width while a total gate-width of 640 μm is used for the second stage. The basic HEMT unit is a four gate-finger device with a total gate-width of 80 μm in common source configuration. Multiple via holes are employed to parallelly connect the HEMT devices in each stage for high output power.

The circuit is designed for high gain and high output power based on reactive matching technique. The matching networks are comprised by cascade high-low impedance microstrip lines on 100-μm-thick GaAs substrate. MIM capacitors are used for dc block and radial stubs are employed for RF by pass. Shunt RC network are used to ensure bias network low-frequency stability. Owing to high transconductance of a large total periphery, isolation resistors are placed between HEMT devices to prevent oscillation. A small resistor is also put in front of a shunt quarter-wave short stub in input matching network to help the out-of-band stability. Four identical Lange couplers are used to form balanced amplifier of both stages. The 3-dB Lange coupler used in this design shows a 0.4-dB amplitude unbalance at 94 GHz via the full-wave EM analysis.

A design procedure using full-wave EM analysis for the passive structures to eliminate the uncertainties due to quasi-static models was incorporated with this W-band monolithic PA design. The design methodology was described in [10]. During the circuit design, extensive EM analyses of matching structures have been performed, and good agreement between circuit simulation and measurement results are observed.

IV. Measurement Results

The PA was first tested for gain via on-wafer measurement. A measured small signal gain of higher than 9 dB is achieved from 93–96 GHz at 4-V drain voltage with gate voltage set to 0 V as shown in Fig. 2. The gain frequency response is peaked at 95 GHz of about 10-dB gain. Both the input and output return losses are better than 10 dB owing to the balanced design using Lange couplers. The PA chip was then tested in a WR-10 waveguide test-fixture for output power performance under the same bias conditions. It demonstrates 20.1-dBm (102 mW) output power with about 6-dB saturated power gain at 94 GHz. The power added efficiency (PAE) is about 8% at output power saturation. This circuit has also been tested over temperatures from −10° to 100°C. The output power versus the input power plots at 94 GHz under various temperature condition are shown in Fig. 3. The small signal gain of at −10°C is increased by about 1 dB compared with

room temperature data and a saturated output power of 110 mW is obtained, while at 100°C we observe about 2-dB gain drop and a saturated output power of 18.6 dBm (73 mW).

A sampling of 37 sites of this PA over six wafers have been tested for small signal gain performance. Out of these 37 circuits, 13 of them showed higher than 7-dB small signal gain from 92–96 GHz, which is equivalent to an RF yield of 37%. The small signal gain histogram for the 37 PA circuits is plotted in Fig. 4. It is noted this yield number is calculated simply by the number of chips meeting the 7-dB gain criteria divided by the number of chips tested without any dc or visual pre-screening. Moreover, if 6-dB gain is used as the screening criteria, the yield become 80% (28 out of 37). Good uniformity from wafer to wafer is also observed. This good yield number indicates the maturity of 0.1-μm power HEMT MMIC technology and the readiness of the MMIC insertion into various W-band systems with high reliability and low cost.

V. Summary

We have presented a monolithic W-band balanced two-stage power amplifier using 0.1-μm AlGaAs/InGaAs/GaAs PM T-gate power HEMT MMIC production process technology. Measurement results show that a small signal gain of 9 dB, an output power of 102 mW, and a PAE of 8% have been achieved at 94 GHz, which rival state-of-the-art performance of the monolithic power amplifiers at this frequency. The success of this W-band monolithic PA indicates the maturity of power HEMT MMIC technology and the readiness of the MMIC insertion into W-band systems with high reliability and low cost.

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